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WHAT IS CLAIMED IS:

1. A non-volatile semiconductor memory device comprising:

a plurality of memory cell arrays each having a plurality of memory cells, said plurality of memory cells being connected to a plurality of word lines;

a plurality of word line drive circuits which are connected to said plurality of memory cell arrays, and which select and drive said plurality of word lines of said corresponding memory cell arrays; and

a plurality of control circuits which are connected to said plurality of memory cell arrays, and execute verifying reading of data which has been written in said plurality of memory cells of the corresponding memory cell arrays, and control a select and drive operation for said word lines in the corresponding word line drive circuit in accordance with a result of the verifying reading.

2. The non-volatile semiconductor memory device according to claim 1, wherein when data is to be written or read, said plurality of memory cell arrays execute parallel writing or reading of data at all of said memory cells which are connected to corresponding word lines in each of said memory cell arrays.

3. The non-volatile semiconductor memory device according to claim 1, wherein, said word line drive circuit corresponding to said control circuit in which

a result of the verifying reading is a pass, is controlled by said control circuit such that the select and drive operation for said plurality of word lines of the corresponding memory cell array is stopped.

4. The non-volatile semiconductor memory device according to claim 1, wherein each of said plurality of memory cells comprises a non-volatile transistor, and said plurality of non-volatile transistors are serially connected to form a NAND cell.

5. The non-volatile semiconductor memory device according to claim 1, wherein each of said plurality of control circuits comprises a plurality of latch circuits which latches data to be read from said plurality of memory cells at the time of the verifying reading.

6. The non-volatile semiconductor memory device according to claim 5, wherein each of said plurality of latch circuits latches write data which is to be written in said plurality of memory cells.

7. The non-volatile semiconductor memory device according to claim 1, wherein each of said plurality of word line drive circuits having a plurality of switches, said plurality of switches are connected between a node of a drive voltage to supply said plurality of word lines and said plurality of word lines, conduction of said plurality of switches are controlled in accordance with control signals output

from said plurality of control circuits.

8. The non-volatile semiconductor memory device according to claim 5, wherein said plurality of control circuits having a plurality of determination circuits, said plurality of determination circuits are connected to said plurality of latch circuits, each of said plurality of determination circuits outputs a determination signal in accordance with a result of a verification based on said data latched at said plurality of latch circuits.

9. The non-volatile semiconductor memory device according to claim 8, wherein said determination circuit comprises:

a first transistor which is connected between a node of a first voltage and a node of said determination signal, conduction of which is controlled at a predetermined timing; and

a plurality of second transistors, each of which is inserted in parallel between said node of said determination signal and a node of a second voltage, conduction of which is controlled based on data latched at said plurality of latch circuits.

10. The non-volatile semiconductor memory device according to claim 9, wherein said determination circuit further comprises:

a plurality of third transistors, each of which is inserted between said plurality of second transistors

and said node of said second voltage, and conduction of which is controlled during a period that said first transistor executes conducting.

11. The non-volatile semiconductor memory device according to claim 8, wherein each of said plurality of control circuits further comprises a storage circuit which stores said determination signal output from said determination circuit.

12. The non-volatile semiconductor memory device according to claim 11, wherein said storage circuit comprises:

a logic circuit which receives said determination signal and outputs said determination signal at a predetermined timing; and

a flip flop circuit which has a set terminal and a reset terminal, output from said logic circuit being input to said set terminal and a reset signal being input to said reset terminal.

13. A non-volatile semiconductor memory device comprising:

a plurality of memory cell arrays each having a plurality of memory cells, said plurality of memory cells being connected to a plurality of word lines;

a plurality of word line drive circuits which are connected to said plurality of memory cell arrays, and which select and drive said plurality of word lines of the corresponding memory cell arrays; and

a plurality of control circuits which are connected to said plurality of memory cell arrays, and which have a plurality of latch circuits which latch write data to be written to said plurality of memory cells of the corresponding memory cell arrays and execute verifying reading of data which has been written in said plurality of memory cells, thereby latching read data, and at a time of data writing, controls a select and drive operation for said word lines in the corresponding word line drive circuit in accordance with write data latched by said plurality of latch circuits, and at a time of verifying reading, controls a select and drive operation for said word lines in the corresponding word line drive circuit in accordance with verifying read data latched by said plurality of latch circuits.

14. The non-volatile semiconductor memory device according to claim 13, wherein when data is to be written or read, said plurality of memory cell arrays execute parallel writing or reading of data at all of said memory cells which are connected to corresponding word lines in each of said memory cell arrays.

15. The non-volatile semiconductor memory device according to claim 13, wherein when all of said write data latched by said plurality of latch circuits are logic data which do not require the write operation to said memory cells, the corresponding word line drive

circuit is controlled by said control circuit such that the select and drive operation for said word lines of the corresponding memory cell is not initiated.

16. The non-volatile semiconductor memory device according to claim 13, wherein when a result is a pass for the verifying reading based on a plurality of verifying read data latched by said plurality of latch circuits, the corresponding word line drive circuit is controlled by said control circuit such that the select and drive operation for said word lines of the corresponding memory cell array is stopped.

17. The non-volatile semiconductor memory device according to claim 13, wherein each of said plurality of memory cells comprises a non-volatile transistor, and said plurality of non-volatile transistors are serially connected to form a NAND cell.

18. The non-volatile semiconductor memory device according to claim 13, wherein each of said plurality of word line drive circuits having a plurality of switches, said plurality of switches are connected between a node of a drive voltage to supply said plurality of word lines and said plurality of word lines, conducting of said plurality of switches are controlled in accordance with control signals output from said plurality of control circuits.

19. The non-volatile semiconductor memory device according to claim 13, wherein said plurality of

control circuits having a plurality of determination circuits, said plurality of determination circuits are connected to said plurality of latch circuits, each of said plurality of determination circuits outputs a determination signal in accordance with a result of a verification based on said data latched at said plurality of latch circuits.

20. The non-volatile semiconductor memory device according to claim 19, wherein said determination circuit comprises:

a first transistor which is connected between a node of a first voltage and a node of said determination signal, and conduction of which is controlled at a predetermined timing; and

a plurality of second transistors, each of which is inserted in parallel between a node of said determination signal and a node of a second voltage, and conduction of which is controlled in accordance with data latched at said plurality of latch circuits.

21. The non-volatile semiconductor memory device according to claim 20, wherein the determination circuit further comprises:

a plurality of third transistors, each of which is inserted between said plurality of second transistors and said node of said second voltage, and conduction of which is controlled during a period that said first transistor executes conducting.

22. The non-volatile semiconductor memory device according to claim 19, wherein each of said plurality of control circuits further comprises a storage circuit which stores said determination signal output from said determination circuit.

23. The non-volatile semiconductor memory device according to claim 22, wherein said storage circuit comprises:

a logic circuit which receives said determination signal and outputs said determination signal at a predetermined timing; and

a flip flop circuit which has a set terminal and a reset terminal, output from said logic circuit being input to said set terminal and a reset signal being input to said reset terminal.

24. A non-volatile semiconductor memory device comprising:

a plurality of memory cell arrays each having a plurality of memory cells, said plurality of memory cells being connected to a plurality of word lines;

a plurality of word line drive circuits which are connected to said plurality of memory cell arrays, and which select and drive said plurality of word lines of the corresponding memory cell arrays; and

a plurality of control circuits which are connected to said plurality of memory cell arrays, and which have a plurality of latch circuits which latch

write data to be written to said plurality of memory cells of the corresponding memory cell arrays, and at a time of data writing, controls a select and drive operation for said word lines in the corresponding word line drive circuit in accordance with write data latched by said plurality of latch circuits, wherein when all of said write data latched by said plurality of latch circuits are logic data which do not require the write operation to said memory cells, the corresponding word line drive circuit is controlled by said control circuit such that the select and drive operation for said word lines of the corresponding memory cell is not initiated.

25. The non-volatile semiconductor memory device according to claim 24, wherein each of said plurality of memory cells comprises a non-volatile transistor, and said plurality of non-volatile transistors are serially connected to form a NAND cell.

26. The non-volatile semiconductor memory device according to claim 24, wherein each of said plurality of word line drive circuits having a plurality of switches, said plurality of switches are connected between a node of a drive voltage to supply said plurality of word lines and said plurality of word lines, conducting of said plurality of switches are controlled in accordance with control signals output from said plurality of control circuits.

27. The non-volatile semiconductor memory device according to claim 24, wherein said plurality of control circuits having a plurality of determination circuits, said plurality of determination circuits are connected to said plurality of latch circuits, each of said plurality of determination circuits outputs a determination signal in accordance with a result of a verification based on said data latched at said plurality of latch circuits.

28. The non-volatile semiconductor memory device according to claim 27, wherein said determination circuit comprises:

a first transistor which is connected between a node of a first voltage and a node of said determination signal, and conduction of which is controlled at a predetermined timing; and

a plurality of second transistors, each of which is inserted in parallel between a node of said determination signal and a node of a second voltage, and conduction of which is controlled in accordance with data latched at said plurality of latch circuits.

29. The non-volatile semiconductor memory device according to claim 28, wherein the determination circuit further comprises:

a plurality of third transistors, each of which is inserted between said plurality of second transistors and said node of said second voltage, and conduction of

which is controlled during a period that said first transistor executes conducting.

30. The non-volatile semiconductor memory device according to claim 27, wherein each of said plurality of control circuits further comprises a storage circuit which stores said determination signal output from said determination circuit.

31. The non-volatile semiconductor memory device according to claim 30, wherein said storage circuit comprises:

a logic circuit which receives said determination signal and outputs said determination signal at a predetermined timing; and

a flip flop circuit which has a set terminal and a reset terminal, output from said logic circuit being input to said set terminal and a reset signal being input to said reset terminal.